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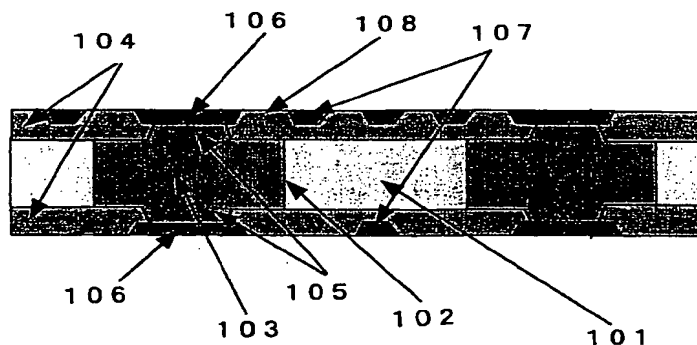
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(54) Printed circuit board and electric components

(57) A printed circuit board has: a base material layer having a first via hole; and an insulating layer having a second via hole, the insulating layer being provided on one surface of the base material layer, wherein a cross-sectional area of the second via hole is smaller

than a cross-sectional area of said first via hole, and wherein the first and second via holes are filled with a conductive material.

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a printed circuit board of two or more layers, and electronic components.

2. Background of the Invention

In recent years, as electronic apparatuses have become smaller and denser, multilayer printed circuit boards being inexpensive and in which semiconductor chips such as LSIs may be mounted at a high density have been strongly demanded not only in the field of industrial apparatuses but also in the field of consumer apparatuses. In such multilayer printed circuit boards, it is important that fine-pitch interconnecting patterns on the layers are electrically connected between the layers with a high degree of reliability.

With respect to this demand, it is extremely difficult to satisfy it by use of conventional printed circuit board manufacturing methods using drilling, etching of copper-coated laminations or plating, so that printed circuit boards having new structures are being developed.

Current representative examples of high-density printed circuit boards include the following:

The first example is a method called a built-up process in which a conventional double-sided or multilayer printed circuit board is used as the core board and insulating layers having smaller via holes and wiring layers being finer are laminated thereon (Susumu Honda "Current State and Problems of Built-up Multilayer Printed Circuit Board Technology", Magazine of Japan Institute for Interconnecting and Packaging Electronic Circuits, Vol. 11, No. 7, pp.462-468 (1996)). According to this method, small holes for smaller via holes are formed in the insulating layers by photoetching or chemical etching by use of a photosensitive insulating material or a chemically etchable material. Recently, methods have been developed which use plasma or a laser to form the holes in the insulating layers. When a laser is used, it is unnecessary for the material to have photosensitivity or chemically etchable property, so that the insulative material may be selected from a wider range.

The second example is a stacking process in which copper foils are laminated on a prepreg with holes filled with a conductive paste (Hiroyuki Okano, "Resin Multilayer Circuit Board with All Layers Having IVH Structure", 1995 Microelectronics Symposium, p.163 (1995)) (generally, this type of circuit board is frequently classified as a built-up multilayer printed circuit board). Researches have been carried out on a circuit board using instead of a prepreg a film having an adhesive (Keiichi Takenouchi et al. "Development of Polyimide Multilayer Circuit Board", Papers Presented at the Tenth

Lecture Meeting on Interconnecting and Packaging Electronic Circuits, pp. 81-82 (1996)).

The third example is a method using a thin film multilayer and is similar to the built-up process described as the first example. This is a thin film multilayer circuit board in which a conventional ceramic multilayer circuit board is used as the core board and on surfaces thereof, inorganic or organic insulating layers and conductive wiring layers patterned by plating and photoetching, etc. are laminated. At present, this method, which uses thin film technology, is the method by which the densest printed circuit boards are manufactured. For the insulating layers, photosensitive polyimide is most frequently used.

However, these printed circuit board manufacturing methods have defects.

According to the built-up process, it is difficult to obtain denser printed circuit boards because a conventional low-density glass epoxy multilayer circuit board is used as the core of the inner layer. In addition, in order to obtain denser printed circuit boards, it is necessary to increase the number of insulating and wiring layers being built up, so that it is technically difficult to flatten the surfaces of printed circuit boards, or the cost increases.

According to the stacking process, it is difficult to form at a low cost the small holes in a prepreg or a film (base material) of a thickness for higher density.

According to the thin film multilayer method which uses a thin film process, the cost is high.

SUMMARY OF THE INVENTION

In view of these problems of the conventional multilayer printed circuit board manufacturing methods, it is an object of the present invention to provide a printed circuit board manufacturing method in which high-density printed circuit boards are easily manufactured at a low cost and a core board having a maximum work size may be used.

To achieve the above-mentioned object, a printed circuit board according to the present invention comprises a base material layer having a first via hole and an insulating layer having a second via hole, said insulating layer being provided on at least one surface of said base material layer, wherein a cross-sectional area of said second via hole is smaller than a cross-sectional area of said first via hole, and wherein said first and second via holes are filled with a conductive material. With these features, fine wiring and fine via hole connection in a printed circuit board having a large work size are enabled, so that low-cost printed circuit boards and electronic components are obtained.

A printed circuit board of the present invention of claim 1 comprises: a base material layer having a first via hole; and an insulating layer having a second via hole, said insulating layer being provided on at least one surface of said base material layer, wherein a cross-

sectional area of said second via hole is smaller than a cross-sectional area of said first via hole, and wherein said first and second via holes are filled with a conductive material.

A printed circuit board of the present invention according to claim 1 is that said conductive material is a conductive paste.

A printed circuit board of the present invention according to claim 2 is that said conductive material with which said first via hole is filled and said conductive material with which said second via hole is filled are the same.

A printed circuit board of the present invention according to claim 2 is that said conductive material with which said first via hole is filled and said conductive material with which said second via hole is filled are different.

A printed circuit board of the present invention according to claim 1 is that said insulating layer is provided on both surfaces of said base material layer.

A printed circuit board of the present invention according to claim 1 is that a wiring portion is provided outside said insulating layer.

A printed circuit board of the present invention according to claim 1 is that a wiring portion is provided inside said insulating layer.

A printed circuit board of the present invention according to claim 7 is that said insulating layer comprises a plurality of layers.

A multilayer printed circuit board of the present invention is that plurality of said printed circuit boards according to any one of claims 1 to 8 are laminated.

A circuit component mount unit of the present is that a circuit component is mounted being connected to said wiring portion on an outermost layer of said printed circuit board according to any one of claims 1 to 8 or to said wiring portion on an outermost layer of said multilayer printed circuit board according to claim 9.

A circuit component mount unit of the present invention according to claim 10 is that said circuit component includes a bare integrated circuit.

An electronic component package of the present invention comprises: a base material layer having a first via hole, said base material having a copper foil pad attached to one surface; an insulating layer having a second via hole, said insulating layer being provided on another surface of said base material; and an electronic component having an electrode so as to correspond to a position of said second via hole, wherein a cross-sectional area of said second via hole is smaller than a cross-sectional area of said first via hole, and wherein said first and second via holes are filled with a conductive material.

An electronic component package of the present invention according to claim 12 is that said conductive material is a copper paste.

An electronic component package of the present invention according to any one of claims 12 to 13 is that

said conductive paste includes an abrasive.

An electronic component package of the present invention according to any one of claims 12 to 14 is that said copper foil pad does not exist, and that said conductive material with which the first and second via holes are filled is solderable.

An electronic component package of the present invention according to any one of claims 12 to 15 is that said insulating layer and said conductive material have flexibility.

An electronic component package of the present invention according to any one of claims 12 to 16 is that said electrode of said electronic component is an aluminum electrode.

A printed circuit board manufacturing method of the present invention comprises;

a first step of forming a wiring layer on an insulating layer having a second via hole; and
a second step of transferring said insulating layer and said wiring layer onto a base material layer having a first via hole filled with a conductive material, said first via hole having a larger cross-sectional area than said second via hole.

A printed circuit board manufacturing method of the present invention according to claim 18 is that said first step, said second via hole is filled with a conductive paste.

A printed circuit board manufacturing method of the present invention comprises a step of laminating an insulating layer on a base material layer and forming a wiring layer on said insulating layer, said base material layer having a first via hole filled with a conductive material, said insulating layer having a second via hole having a smaller cross-sectional area than said first via hole.

An electronic component package manufacturing method of the present invention comprises the steps of:

forming an insulative resin layer on a surface of an electronic component having a predetermined electrode on said surface;
forming a through hole in said insulative resin layer so as to correspond to a position of said electrode;
embedding a conductive paste into said through hole; and
heating and pressurizing said insulative resin layer filled with said conductive paste to thereby paste said insulative resin layer to said electronic component.

An electronic component package manufacturing method of the present invention according to claim 21 is that said conductive paste is a copper paste.

An electronic component package manufacturing method of the present invention according to claim 21, 22 or 23 is that said conductive paste includes an abra-

sive.

An electronic component package manufacturing method of the present invention according to claim 21, 22 or 23 is that said insulative resin layer has a compressibility.

An electronic component package manufacturing method of the present invention according to claim 24 is that said insulative resin layer is a prepreg with aramid nonwoven cloth as a reinforcing material.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view of a double-sided printed circuit board according to an embodiment of the present invention;

FIG. 2 is a cross-sectional view of a double-sided printed circuit board in which wiring layers are provided inside insulating layers in the embodiment of the present invention;

FIG. 3 shows an embodiment in which the insulating layer is provided only on one surface of a base material in the embodiment of the present invention;

FIG. 4 is a cross-sectional view of a multilayer printed circuit board (four-layer printed circuit board) according to an embodiment of the present invention;

FIG. 5 shows a circuit component mount unit using a circuit board of an embodiment of the present invention manufactured by a transfer process;

FIG. 6 shows another embodiment of the multilayer printed circuit board of the present invention;

FIG. 7 shows an example of a transfer medium according to an embodiment of the present invention;

FIG. 8 shows an example of a transfer process according to an embodiment of the present invention;

FIG. 9 shows an example of a transfer medium according to an embodiment of the present invention;

FIG. 10 is a cross-sectional view of a double-sided printed circuit board manufactured by using the transfer medium of FIG. 9;

FIG. 11 shows a flexible printed circuit board used for an embodiment of the present invention;

FIG. 12 is a cross-sectional view of a double-sided circuit board according to an embodiment of the present invention using the flexible printed circuit board;

FIG. 13 shows an example of a built-up process according to an embodiment of the present invention;

FIG. 14 shows a copper foil having an insulating layer, used in an embodiment of the present invention;

FIG. 15 shows a process using the copper foil of FIG. 14;

FIG. 16 shows an example of a method for manufacturing a multilayer printed circuit board according to an embodiment of the present invention;

FIG. 17 shows a transfer medium according to an embodiment of the present invention;

FIG. 18 shows a double-sided printed circuit board manufactured by preparing two of the transfer media shown in FIG. 17;

FIG. 19 shows an example of a small-size package such as a semiconductor chip according to an embodiment of the present invention;

FIG. 20 is a perspective view of the package of FIG. 19; and

FIG. 21 shows another example of a small-size package such as a semiconductor chip according to an embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMOBIMENTS

Embodiments of the present invention will hereinafter be described with reference to the drawings.

(First Embodiment)

FIG. 1 is a cross-sectional view of a double-sided printed circuit board according to a first embodiment of the present invention. A base material layer 101 with a first via hole 103 is provided and an insulating layer 104 with a second via hole 105 having a smaller cross-sectional area than the first via hole is provided on each surface of the base material layer 101. Above the via hole 105, a via pad 106 is provided. Reference numeral 107 represents a wiring. The wiring and the via pad constitute a wiring layer. The upper and lower wiring layers 107 are electrically connected by the first via hole 103 and the second via hole 105 and constitute a double-sided printed circuit board as a whole.

Since the circuit board has such a structure, the cross-sectional area of the second via hole 105 may be small. Moreover, although the wiring 107 is formed on the insulating layer 104, since the second via hole 105 is small in size, the via pad 106 thereof may be small, so that even if the first via hole 103 has a large cross-sectional area, a fine (high-density) printed circuit board is obtained irrespective of the cross-sectional area of the first via hole 103. Consequently, short circuit with the first and second via holes 103 and 105 does not occur even if a wiring interval 108 is small. In addition, since the cross-sectional area of the first via hole 103 may be large as mentioned above, manufacture of printed circuit boards is facilitated.

It is preferred for the base material layer 101 to be electrically insulative and have a mechanical strength necessary as a circuit board. A glass epoxy board comprising hardened epoxy resin with glass fibers as a reinforcing material or an aramid epoxy board comprising hardened epoxy resin with aramid fibers as a reinforcing material may be used. Known resins may be used which

have been developed for printed circuit boards.

A via hole 102 comprising the first via hole 103 and the second via hole 105 is filled with a conductive material. As the conductive material, a hardened conductive paste in which copper powder or silver powder is mixed in resin, or gold, silver, copper, lead, etc. or an alloy thereof may be used.

The conductive material with which the first via hole 103 is filled and that with which the second via hole 105 is filled may be the same or may be different. Different materials are preferable for filling the via holes having different diameters to each other.

While the wiring layers 107 are formed outside the insulating layers 104 in FIG. 1, as shown in FIG. 2, insulating layers 202 may be provided outside a double-sided circuit board 201 of FIG. 1 so that the wiring layers 107 are situated inside the overall insulating layer (comprising the insulating layers 104 and the insulating layers 202). The structure shown in FIG. 2 is effective when multilayer printed circuit boards are manufactured. Holes 203 formed in the surfaces serve as via holes for connection to upper and lower layers. The cross-sectional area of the hole 203 may be freely decided. When insulating layers are used as the surface layers, the insulating layers 202 are solder resist layers. Methods for manufacturing the printed circuit boards of the structures of FIGs. 1 and 2 will be described later.

FIG. 3 shows an embodiment in which an insulating layer 304 is provided only on one surface of a base material layer 301. Reference numeral 303 represents a first via hole. Reference numeral 305 represents a second via hole having a small cross-sectional area. Via pads 306 and wirings 307 constitute wiring layers. Since the insulating layer 304 prevents the wirings 307 from short-circuiting with the first via hole 303 having a large cross-sectional area, fine wiring is enabled.

The provision of the insulating layers like in the above-described examples not only enables fine wiring but also is effective for ensuring the adhesive strength of the wirings 307.

FIG. 4 shows a cross-sectional view of a multilayer printed circuit board (four-layer printed circuit board) according to the present invention. Two double-sided printed circuit boards 401 are the same as the one described with reference to FIG. 2. The two double-sided printed circuit boards 401 are mechanically and electrically connected through a base material 402 having a via hole 403. The via hole 403 comprises a first via hole 404 provided in the base material 402 and a via hole 405 provided in an insulating layer 406 and having a smaller cross-sectional area than the first via hole 404. As the materials for the base material and the via holes, the same ones as those described with reference to FIG. 1 may be used.

As the upper and lower double-sided printed circuit boards 401, it is not always necessary to use double-sided printed circuit boards of a structure according to the present invention. As an example, FIG. 6 shows a

cross-sectional view of a four-layer printed circuit board in which a printed circuit board structure according to this embodiment is applied to two conventional double-sided printed circuit boards. Reference numeral 501 represents conventional via hole glass epoxy double-sided printed circuit boards. Wirings 512 on both surfaces are electrically connected by a via hole 511. While an inside 510 of the via hole is typically empty, the via hole 511 is filled with resin in this example. Two conventional double-sided circuit boards 501 are mechanically and electrically connected through a base material 502 having a via hole 503. The via hole 503 comprises a first via hole 504 provided in the base material 502 and a via hole 505 provided in an insulating layer 506 and having a smaller cross-sectional area than the first via hole 504. As the materials for the base material and the via holes, the same ones as those described with reference to FIG. 1 may be used.

While four-layer printed circuit boards were described with reference to FIGs. 4 and 6, it is to be understood that the present invention is not limited thereto. More layers may be laminated in a similar structure.

Methods for manufacturing the printed circuit boards according to the above-described embodiments of the present invention will be described.

First, a manufacturing method using transfer technology will be described. This method uses a transfer medium as shown in FIG. 7. On a surface of a supporter 601 with the surface processed so as to be peelable, a wiring layer is formed such as the wiring 107 including the via pad 106. The formation is performed through a wiring forming process using plating, evaporation and photoprocess. On the wiring layer, the insulating layer 104 is formed having a hole 602 which is to serve as the second via hole. A transfer medium 603 thus structured is prepared. Specifically, a copper pattern formed by plating is formed on a supporter made of stainless steel.

Two of such transfer media are prepared and an unhardened base material 701 having a hole which is to serve as the first via hole and is filled with a conductive paste 702 is sandwiched between the transfer media as shown in FIG. 8. Then, the lamination is pressurized and heated in a vacuum (FIG. 8A) to harden the conductive paste and the base material for integration. Then, the supporters are peeled off (FIG. 8B). As the unhardened base material 701, for example, an aramid epoxy prepreg may be used, which is aramid nonwoven cloth pregnant with epoxy resin. As the conductive paste, copper paste may be used. The holes may be formed by a laser or may be mechanically formed by a drill. With respect to the size of the holes, when the unhardened base material is approximately 150 μ m in thickness, holes of approximately 100 μ m to 300 μ m are easy to form. The aramid epoxy prepreg which has a multiplicity of cavities inside is compressed when pressurized and heated, so that the base material decreases in thickness as shown in FIG. 8B. At this

time, the copper paste and the first via hole constitute the second via hole. In actuality, there are occasions when the copper paste is squeezed out at portions 703 of FIG. 8. The conductive paste 702 may be provided so as to protrude from the surface of the prepreg.

Another method is such that a cone-shaped protrusion comprising hardened conductive paste is formed on the lower-side second via hole and the protrusion conductor is connected with the upper-side second via hole penetrating through a base material made of softened resin.

While an aramid epoxy prepreg is used as the unhardened base material in the above-described example, the present invention is not limited thereto. For example, a sheet comprising an insulative film coated with an adhesive may be used, or a sheet-form unhardened adhesive may be used. The conductive paste is not limited to copper paste. For example, conductive paste of gold, silver or carbon, etc. may be used.

Moreover, it is unnecessary that the first via hole be filled with only the conductive paste. For example, a metallic ball may be embedded in the hole so that the electric connection is made by the conductive paste with which the second via hole is filled.

When the wiring 107 and the via pad 106 of FIG. 7 are necessarily fine, they may be formed by the additive process. That is, a patterned plating resist layer is formed on a surface of the supporter 601 before plating, and a plating film is deposited on the exposed portion of the conductive supporter. According to this method, a pattern is obtained which is fine and has a large film thickness. The wiring and the via pad may be formed by printing conductive paste. This is a very easy method. In the case where pressurizing and heating are performed at the time of the transfer, the conductivity is higher than in the case where hardening is performed only by heating.

By using a transfer medium as shown in FIG. 9, the electrical connection between the first via hole and the second via hole is ensured. Reference numeral 801 represents a conductive paste with which the second via hole is filled. The conductive paste 801 may be formed by printing. Needless to say, it may be formed by use of plating and patterning technology. In the case of using the transfer medium as FIG. 9, the difficulty of flowing of the conductive paste into the small second via hole is more eliminated in comparison with the transfer medium of FIG. 7. FIG. 10 is a cross-sectional view of a double-sided printed circuit board manufactured by using the transfer medium of FIG. 9. While the conductive material of the first via hole and that of the second via hole are different in this circuit board, it is needless to say that they may be the same. In FIG. 10, the upper and lower patterns on the double-sided printed circuit board are shifted from each other in position. This indicates that the position alignment of the upper and lower patterns may be rough in this embodiment. That is, since a big first via hole may be formed in this embodi-

ment, the condition of the connection is excellent even if the patterns are somewhat shifted from each other in position. Since the patterns may be somewhat shifted from each other in position, it is enabled to form a circuit board having a large work size and obtain products by dividing it in the last place (while via holes tend to shift from each other in position in a circuit board having a large work size, a sufficiently large work size may be provided in a circuit board in which the connection is ensured even if the via holes are somewhat shifted from each other in position like in this embodiment). Thus, the present invention produces an advantage that a circuit board may be manufactured in which the work size is large although the patterns and the via holes are fine.

Next, flexible-printed-circuit method as another manufacturing method according to the present invention will be described. FIG. 11 shows a flexible printed circuit board comprising an insulating layer 1001 and a wiring 1002. The insulating layer 1001 comprises a film, and a polyimide film is most frequently used therefor. The wiring 1002 comprises a copper foil patterned by photoetching. A hole 1003 is to serve as the second via hole. This hole is easily formed by using an excimer laser. The circuit board of this structure has been well known as a TAB tape aside from the size of the holes. FIG. 12 shows a cross-sectional view of a double-sided printed circuit board according to this embodiment using the flexible printed circuit board.

Next, FIG. 13 shows a built-up process as a manufacturing method according to the present invention in which layers are successively laminated on a base material. In this process, a base material 1201 having already been hardened is used which has a first via hole 1202 having already been hardened. An insulating layer 1204 having a second via hole 1203 is formed on each of the upper and lower surfaces of the base material 1201 and a wiring 1205 is formed by plating or another conductive film forming method. In this structure, the conductive material with which the second via hole is filled is different from that with which the first via hole is filled.

The processes shown in FIGs. 14 and 15 resemble the flexible-printed-circuit method but the order of manufacturing steps is different. As shown in FIG. 14, upper and lower insulating layers 1303 each having a hole 1302 which is to serve as the second via hole are prepared on copper foils 1301 and an unhardened base material in which a hole that is to serve as the first via hole is filled with an unhardened conductive paste is interposed therebetween. The lamination is pressurized and heated to harden the base material and the conductive paste for integration (FIG. 15A). Then, the copper foils on the surfaces are patterned by etching to obtain a double-sided circuit board (FIG. 15B).

FIG. 16 shows a method for manufacturing a multi-layer printed circuit board. Two double-sided printed circuit boards 1501 as described with reference to FIG. 2 are prepared and an unhardened base material 1502 in

which a hole that is to serve as the first via hole is filled with a conductive paste is sandwiched therebetween. The lamination is pressurized and heated in a vacuum (FIG. 16A) so that the conductive paste and the base material are hardened for integration (FIG. 16B). Thus, a four-layer printed circuit board is manufactured. It is easy to manufacture a printed circuit board comprising more layers and the printed circuit board is doubled-sided. By laminating one more layer of the double-sided printed circuit board on each surface, a six-layer printed circuit board is realized and by laminating two four-layer printed circuit boards, an eight-layer printed circuit board is realized.

The transfer medium shown in FIG. 17 is a transfer medium effective for manufacturing a double-sided printed circuit board according to another mode. A mold release treatment is applied to a surface of a supporter 1601 and an insulating layer 1602 is formed on the surface. Then, a necessary hole 1606 is formed and a wiring 1603 comprising a conductive film is laminated. Then, a hole 1605 which is to serve as the second via hole is formed. The transfer medium is thus formed. By preparing two such transfer media and manufacturing a double-sided printed circuit board in a manner similar to that described with reference to FIG. 7, one as shown in FIG. 18 is realized. The surfaces of the double-sided circuit board are flat.

FIG. 5 shows a circuit component mount unit using a circuit board according to the present invention manufactured by the transfer process. Reference numeral 407 represents a bare chip. Reference numeral 408 represents a bump. Reference numeral 409 represents an under fill. Reference numeral 410 represents the multilayer printed circuit board of FIG. 4. The circuit component mounted unit is inexpensive although being high in density and small in size because the surfaces of the printed circuit board are flat, and then there are no solder bridges and the yield is excellent. In particular, a circuit component mounted unit in which a bare LSI is flip-chip-bonded onto a printed circuit board according to the present invention is small in size, high in speed and inexpensive.

FIG. 19 is a cross-sectional view of a package of electronic components such as semiconductor chips according to another embodiment of the present invention. The following are laminated from the top to the bottom: a base material layer 1704 having a copper foil pad 1706 on its one surface and having a first via hole 1707; an insulating layer 1703 having a second via hole 1708 and provided on the other surface of the base material layer 1704; and a semiconductor chip 1701 having an electrode 1702 so as to correspond to the position of the second via hole 1708. The cross-sectional area of the second via hole 1708 is smaller than that of the first via hole 1707. The first and second via holes are filled with a conductive material 1705. An input and output pad (electrode) 1702 is typically an aluminum electrode in the case of the semiconductor chip. The base material

layer 1704 is made of an insulative resin. The insulating-cum-protective film 1703 is an insulating-cum-protective film on the semiconductor chip and is typically made of silicon nitride. Recently, a silicon nitride film coated with polyimide has been frequently used.

As the insulative resin for the base material layer, many resins are known now. Epoxy resin is widely used in this field. Some resins are provided with photosensitivity for the formation of the holes. The range of choice of resin has been extended because the laser can now be used for forming the holes. As the resin used for electronic components, one which is low in moisture absorbency is desired. Such resins have been developed in multiplicity. Moreover, as the resin which is in contact with the semiconductor, one which is low in impurity content is preferred. Although the thermal expansion coefficient is preferably close to that of silicon, since there is no simple material that has such a thermal expansion coefficient, a filler is frequently mixed.

For excellent electrical connection between the aluminum electrode and the conductive material, it is necessary to remove an oxide film on the surface of the aluminum electrode. Before the conductive paste is brought into contact with the aluminum electrode, the oxide film on the aluminum surface is removed by reverse sputtering or reduction treatment.

The package of FIG. 19 has the same size as the semiconductor chip, and is low in cost because it is small in size and easily manufactured.

FIG. 21 shows another example of the package. When the conductive paste 1705 is of a solderable type, the package may be treated as a package mountable on a printed circuit board under the condition of FIG. 21. FIG. 20 is a perspective view of the printed circuit board of FIG. 19 viewed from the bottom surface side.

As the solderable conductive paste 1705, a conductive paste is preferred which comprises copper powder, resin and a hardener. The content of the copper powder is preferably 85 weight % or higher. A conductive paste is commercially available which is solderable without any treatment applied thereto after hardening. Even when normal copper paste is used, soldering is enabled by mechanically or chemically removing the resin on the surface after hardening. As a simple method therefor, soldering is enabled by mechanically grinding the surface.

The present invention does not stick to soldering. Recently, an attempt has frequently been made to bond electronic components to a printed circuit board with a conductive paste without the use of solder in order to prevent lead pollution. This package conforms to this tendency.

Simple methods for manufacturing a package of the structure of FIG. 19 or FIG. 21 include a method in which a through hole is formed in an insulative resin sheet in a position corresponding to the position of the electrode of an electronic component, a conductive

paste is embedded in the hole and pressurized and heated so that the conductive paste is hardened to bond the electronic component.

At this time, by using as the insulative resin sheet a prepreg with aramid nonwoven cloth as a reinforcing material, the conductive paste is compressed at the time of heating and pressurizing because of its compressibility, so that the conductivity increases after the paste is hardened. Needless to say, a simple resin may be used as the insulative resin sheet. Since the resin flows at the time of heating and pressurizing, similar effects to those of a compressive insulative resin sheet are obtained. The pressurizing process is important. Moreover, since the oxide film on the aluminum electrode can be broken by the pressurizing process, the oxide film removing process to be performed in advance may be omitted. In order to positively use this effect, it is also preferred to mix abrasive particle in the conductive paste.

It should be understood that the package of this structure may be processed not in chips but in wafers. A pretreatment is performed before the wafer is divided into chips and the wafer is divided later. Consequently, the cost of the package is greatly reduced. It is apparent that the method for manufacturing the structure of the present invention is not limited to the above-described manufacturing methods. There are many other available manufacturing methods. An example is a method in which a semiconductor wafer is coated with an insulative resin, the insulative resin is hardened by heating, a through hole is formed in the insulative resin with an excimer laser so that an aluminum electrode is exposed, the hole is filled with a conductive paste, the conductive paste is heated and pressurized and the surface is ground.

As is apparent from the above-described embodiments, the present invention provides a circuit board comprising a base material layer having a first via hole and an insulating layer having a second via hole and provided on at least one surface of the base material layer, and being inexpensive because a fine interconnecting pattern may be formed and the work size may be large although the first via hole is large since the cross-sectional area of the second via hole is smaller than that of the first via hole. In addition, a package is obtained which is inexpensive because treatments may be performed in wafers.

Claims

1. A printed circuit board comprising: a base material layer having a first via hole; and an insulating layer having a second via hole, said insulating layer being provided on at least one surface of said base material layer, wherein a cross-sectional area of said second via hole is smaller than a cross-sectional area of said first via hole, and wherein said first and second via holes are filled with a conduc-

tive material.

2. A printed circuit board according to claim 1, wherein said conductive material is a conductive paste.
3. A printed circuit board according to claim 2, wherein said conductive material with which said first via hole is filled and said conductive material with which said second via hole is filled are the same.
4. A printed circuit board according to claim 2, wherein said conductive material with which said first via hole is filled and said conductive material with which said second via hole is filled are different.
5. A printed circuit board according to claim 1, wherein said insulating layer is provided on both surfaces of said base material layer.
6. A printed circuit board according to claim 1, wherein a wiring portion is provided outside said insulating layer.
7. A printed circuit board according to claim 1, wherein a wiring portion is provided inside said insulating layer.
8. A printed circuit board according to claim 7, wherein said insulating layer comprises a plurality of layers.
9. A multilayer printed circuit board wherein a plurality of said printed circuit boards according to any one of claims 1 to 8 are laminated.
10. A circuit component mount unit wherein a circuit component is mounted being connected to said wiring portion on an outermost layer of said printed circuit board according to any one of claims 1 to 8 or to said wiring portion on an outermost layer of said multilayer printed circuit board according to claim 9.
11. A circuit component mount unit according to claim 10, wherein said circuit component includes a bare integrated circuit.
12. An electronic component package comprising: a base material layer having a first via hole, said base material having a copper foil pad attached to one surface; an insulating layer having a second via hole, said insulating layer being provided on another surface of said base material; and an electronic component having an electrode so as to correspond to a position of said second via hole, wherein a cross-sectional area of said second via

hole is smaller than a cross-sectional area of said first via hole, and wherein said first and second via holes are filled with a conductive material. *

13. An electronic component package according to claim 12, wherein said conductive material is a copper paste. 5
14. An electronic component package according to any one of claims 12 to 13, wherein said conductive paste includes an abrasive. 10
15. An electronic component package according to any one of claims 12 to 14, wherein said copper foil pad does not exist, and wherein said conductive material with which the first and second via holes are filled is solderable. 15
16. An electronic component package according to any one of claims 12 to 15, wherein said insulating layer and said conductive material have flexibility. 20
17. An electronic component package according to any one of claims 12 to 16, wherein said electrode of said electronic component is an aluminum electrode. 25
18. A printed circuit board manufacturing method comprising: 30
 - a first step of forming a wiring layer on an insulating layer having a second via hole; and
 - a second step of transferring said insulating layer and said wiring layer onto a base material layer having a first via hole filled with a conductive material, said first via hole having a larger cross-sectional area than said second via hole. 35
19. A printed circuit board manufacturing method according to claim 18, wherein in said first step, said second via hole is filled with a conductive paste. 40
20. A printed circuit board manufacturing method comprising a step of laminating an insulating layer on a base material layer and forming a wiring layer on said insulating layer, said base material layer having a first via hole filled with a conductive material, said insulating layer having a second via hole having a smaller cross-sectional area than said first via hole. 45 50
21. An electronic component package manufacturing method comprising the steps of: 55

forming an insulative resin layer on a surface of an electronic component having a predetermined electrode on said surface;

forming a through hole in said insulative resin layer so as to correspond to a position of said electrode;

embedding a conductive paste into said through hole; and

heating and pressurizing said insulative resin layer filled with said conductive paste to thereby paste said insulative resin layer to said electronic component.

22. An electronic package manufacturing method according to claim 21, wherein said conductive paste is a copper paste.
23. An electronic component package manufacturing method according to claim 21, 22 or 23, wherein said conductive paste includes an abrasive.
24. An electronic component package manufacturing method according to claim 21, 22 or 23, wherein said insulative resin layer has a compressibility.
25. An electronic component package manufacturing method according to claim 24, wherein said insulative resin layer is a prepreg with aramid nonwoven cloth as a reinforcing material.

Fig. 1

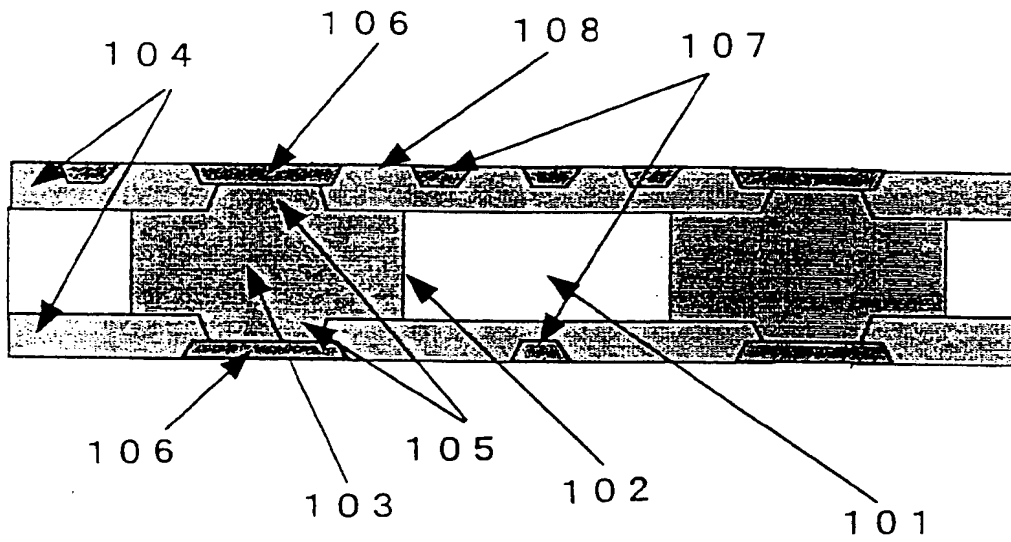


Fig. 2

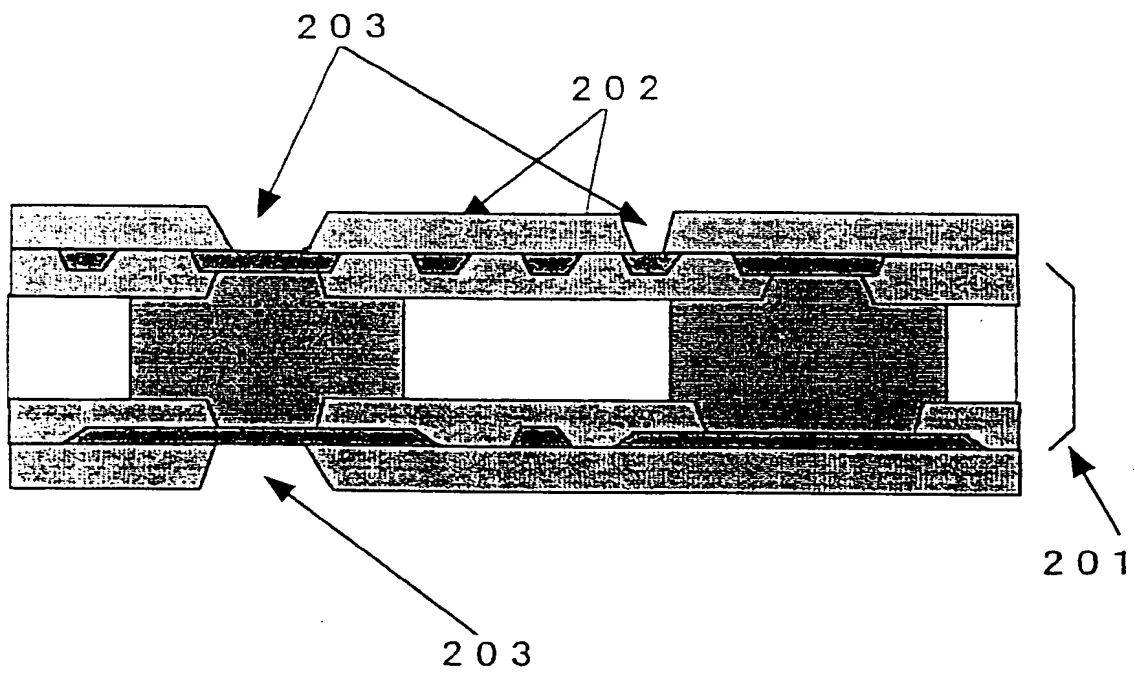


Fig. 3

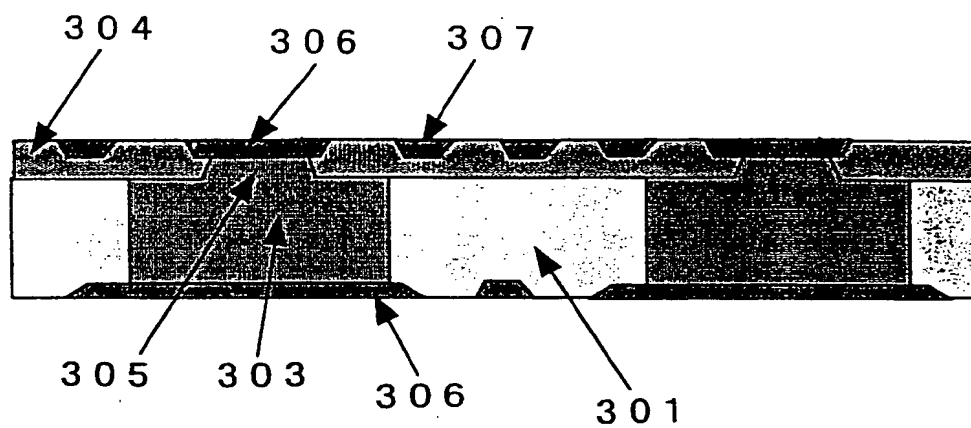


Fig. 4

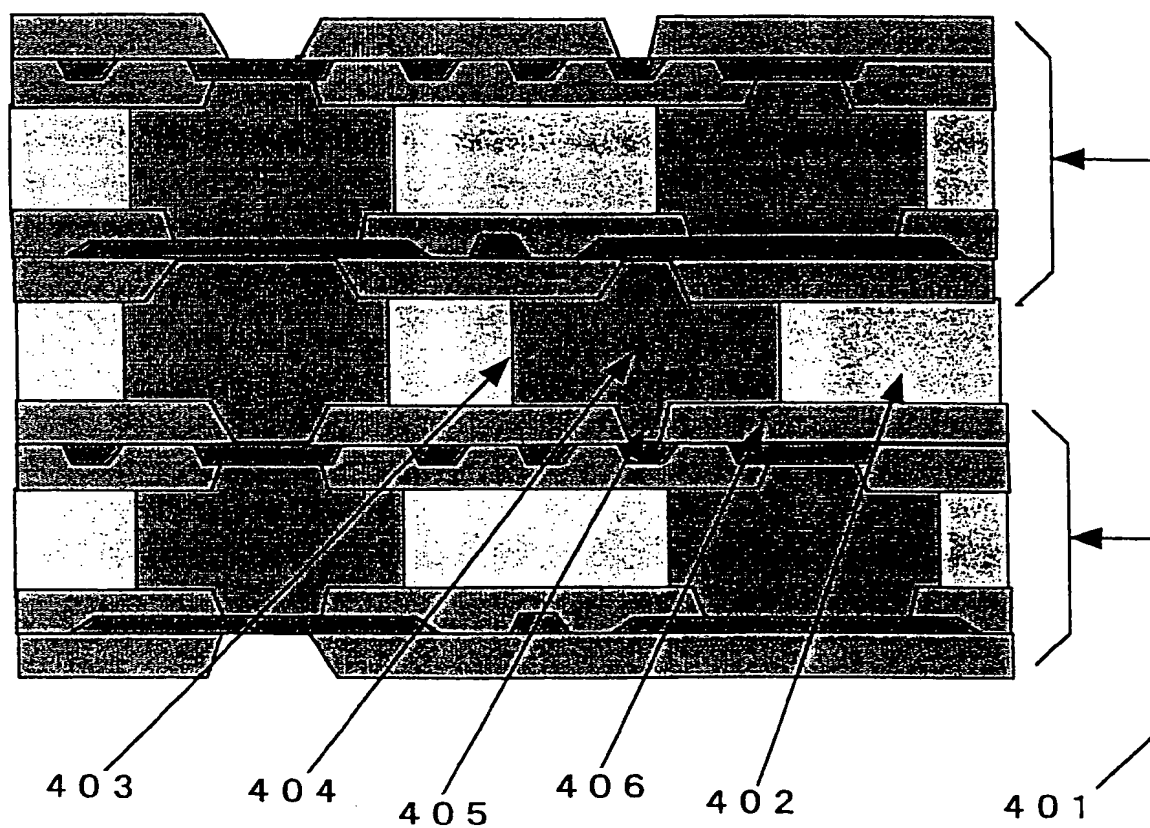


Fig. 5

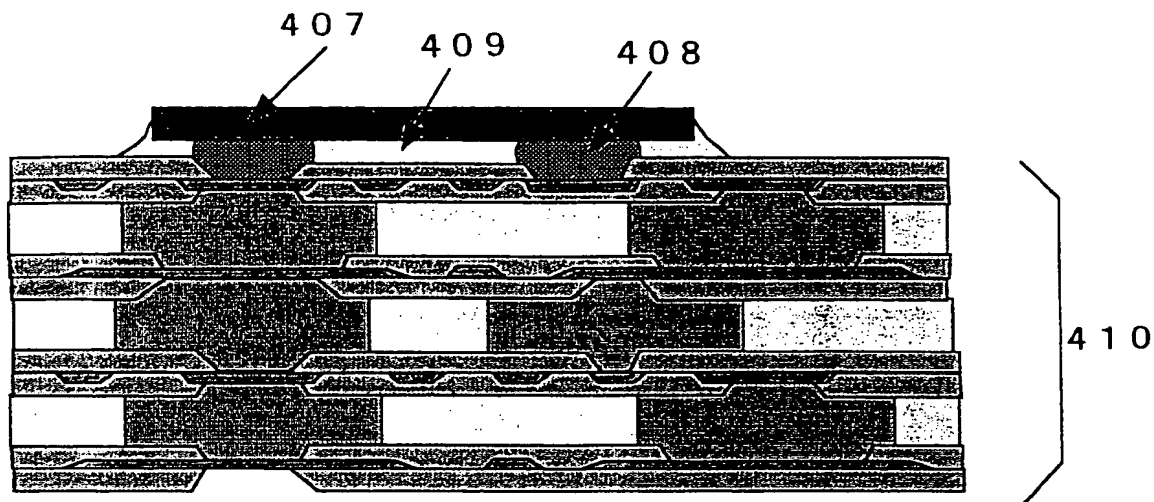


Fig. 6

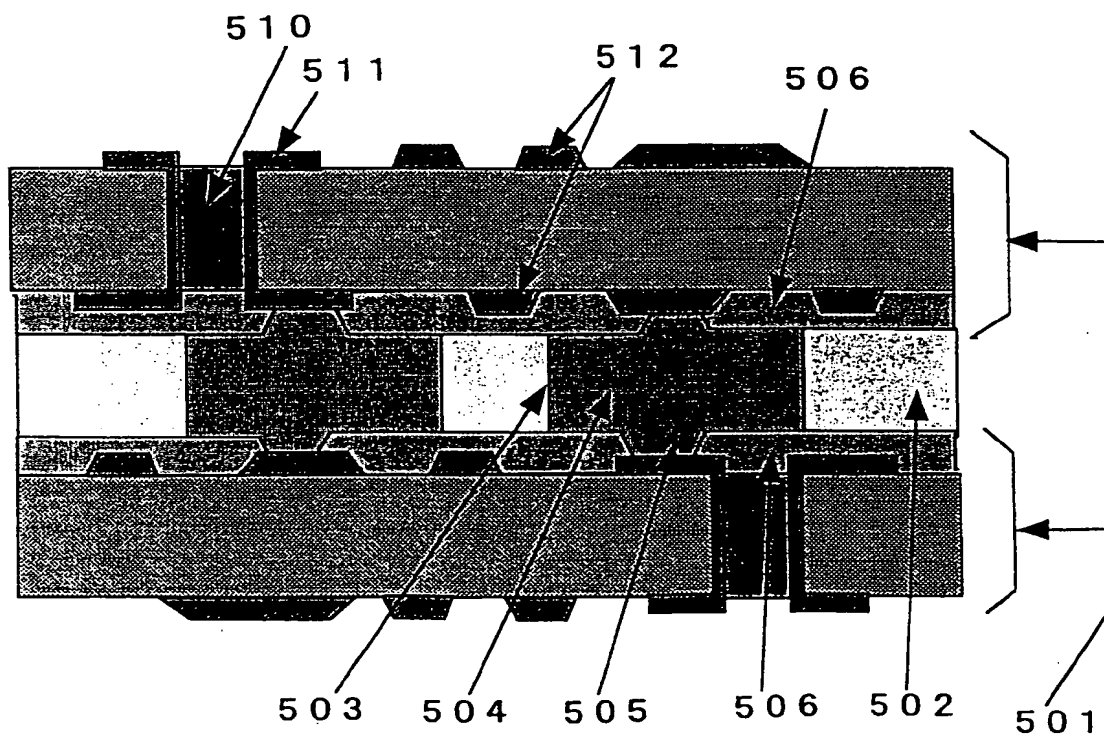


Fig. 7

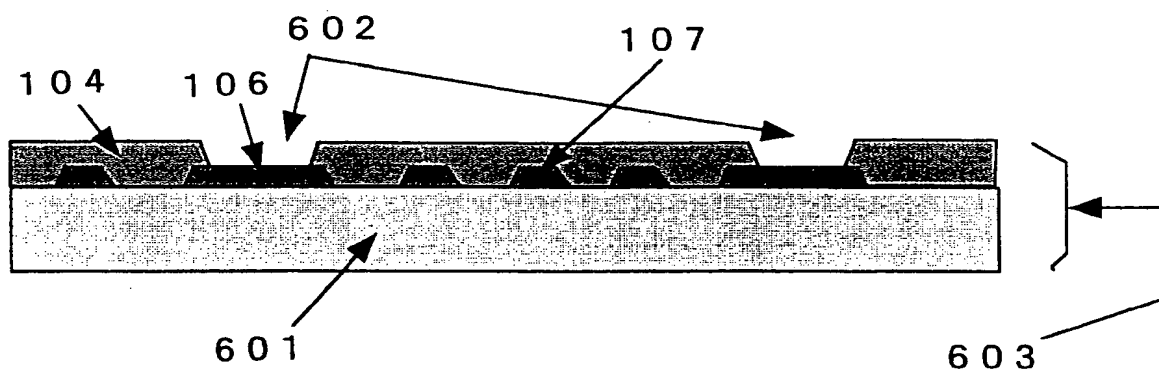


Fig. 9

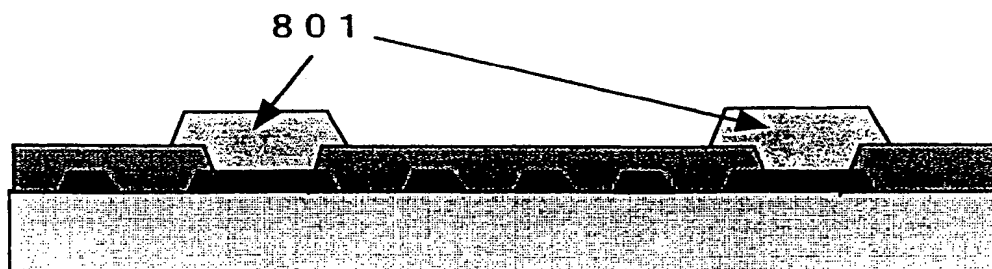


Fig. 8 A

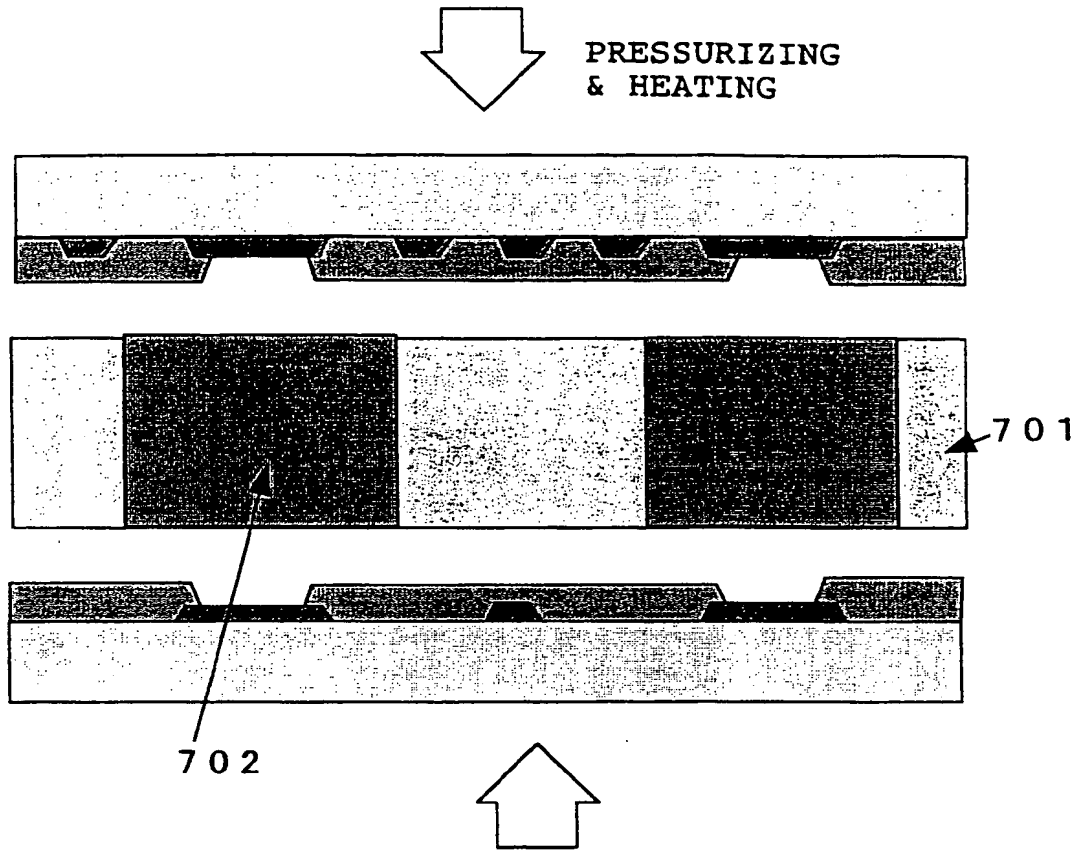
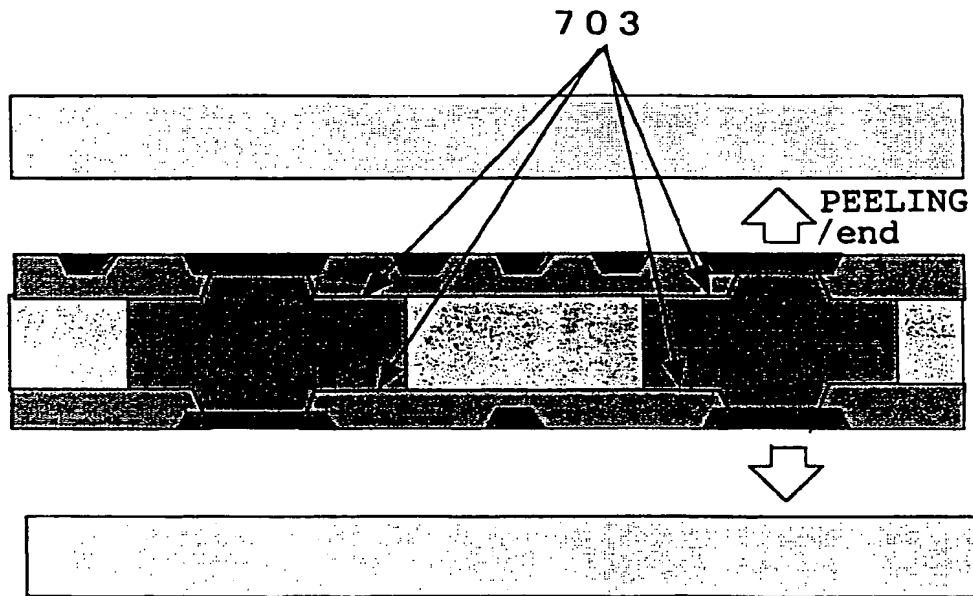
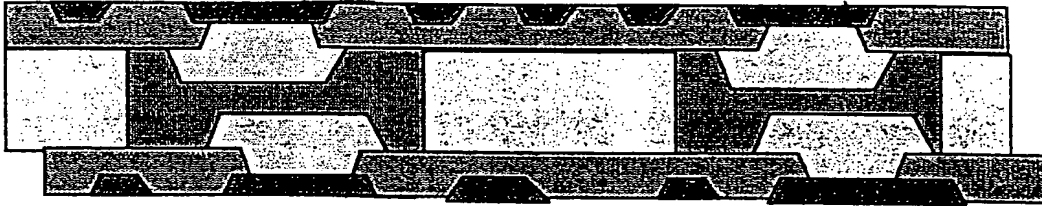


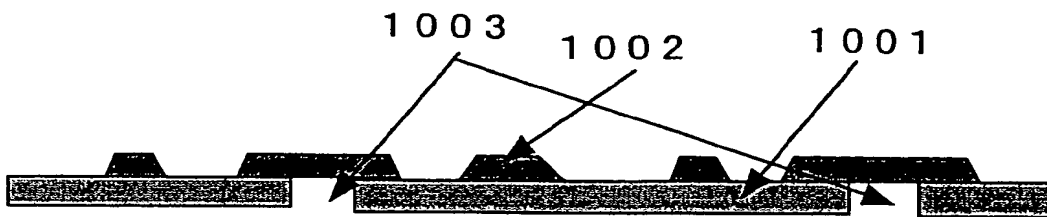
Fig. 8 B



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F i g . 1 1



F i g . 1 2

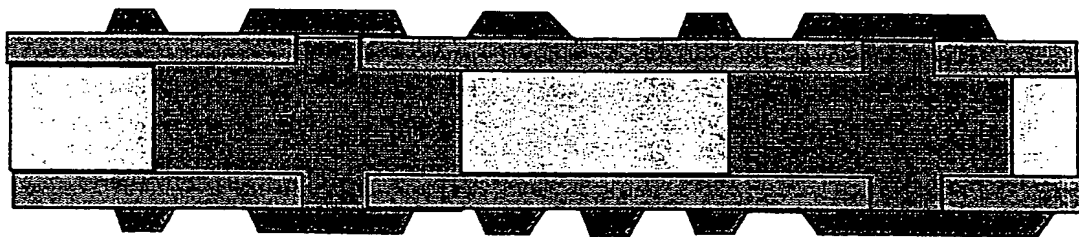


Fig. 13 A



Fig. 13 B

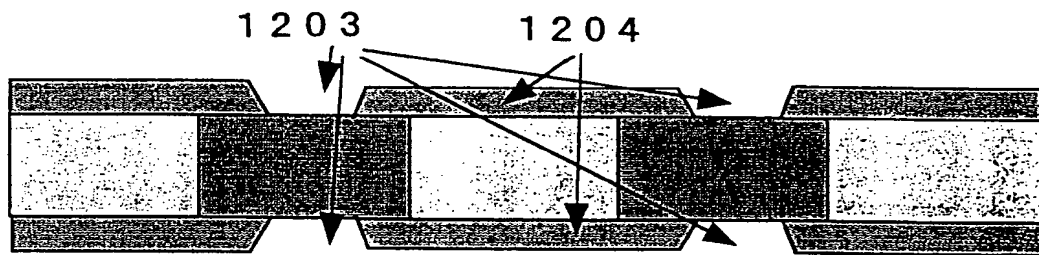


Fig. 13 C

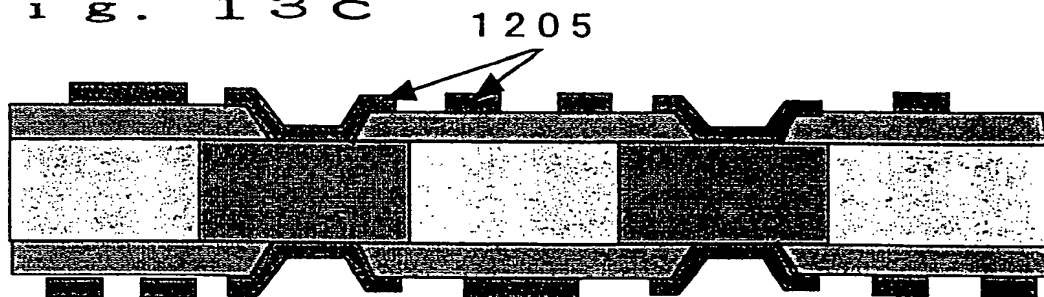


Fig. 14

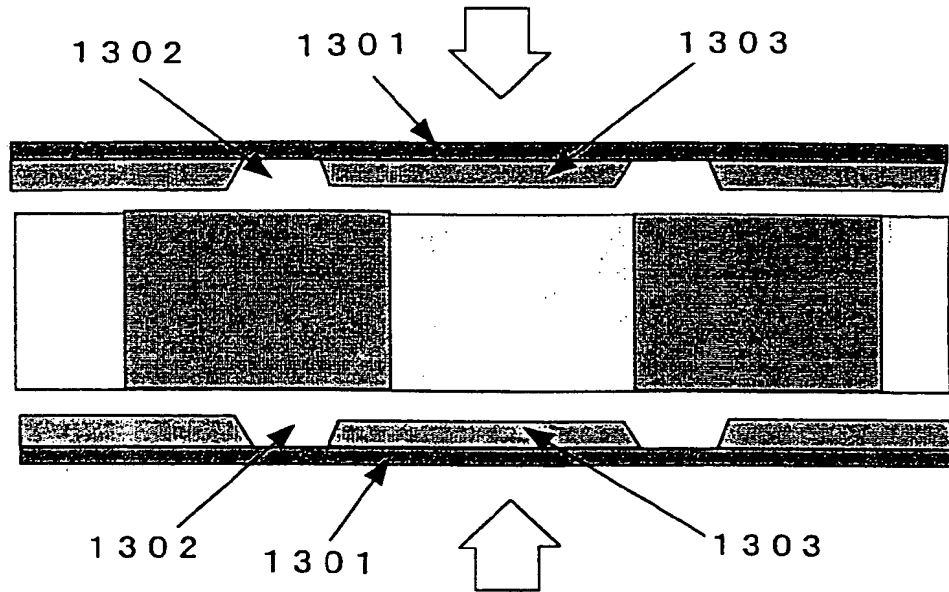


Fig. 15 A

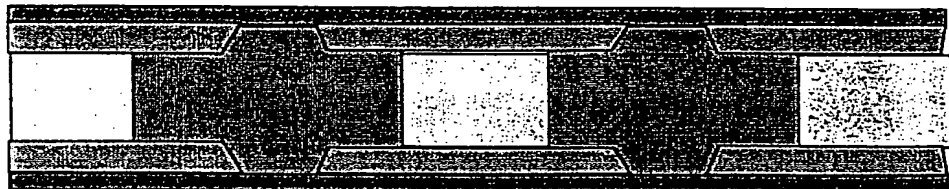


Fig. 15 B

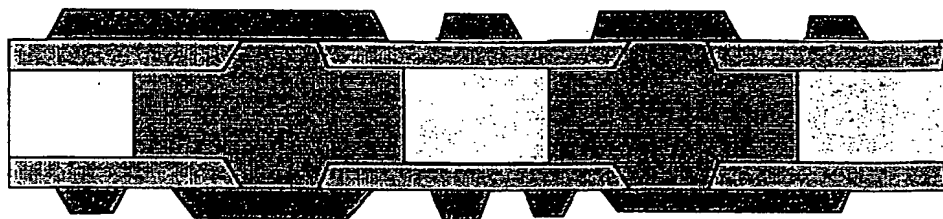


Fig. 16 A

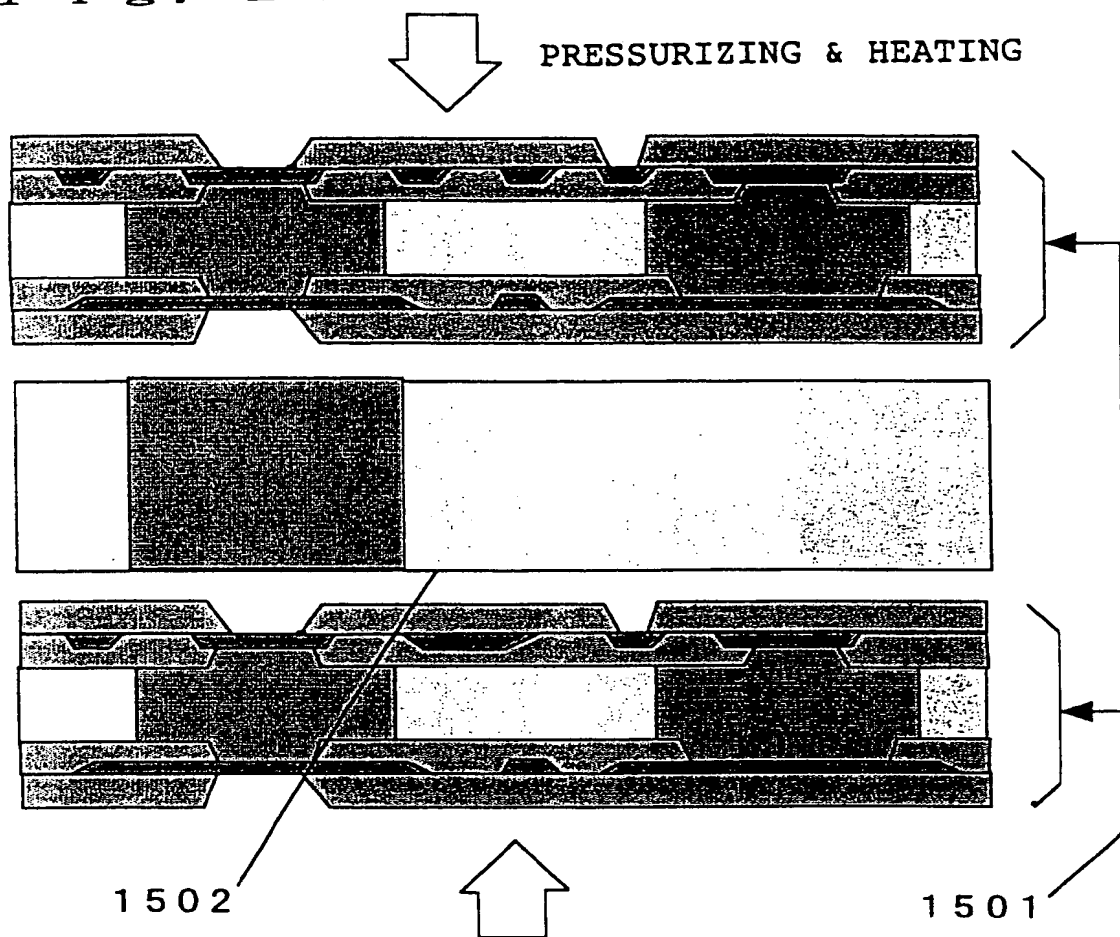


Fig. 16 B

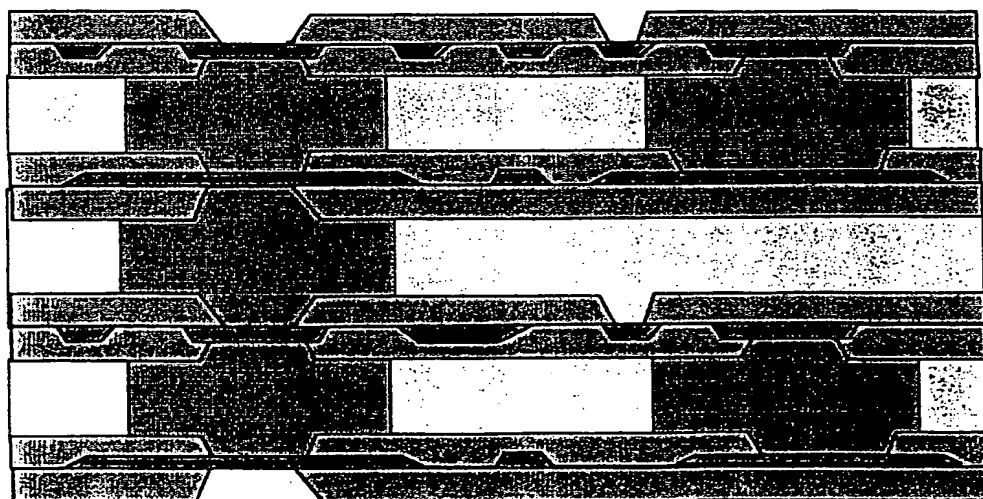


Fig. 17

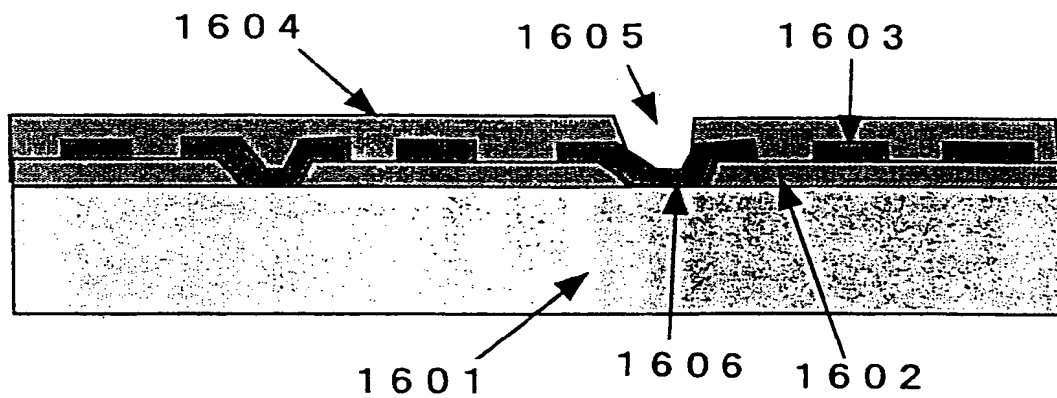
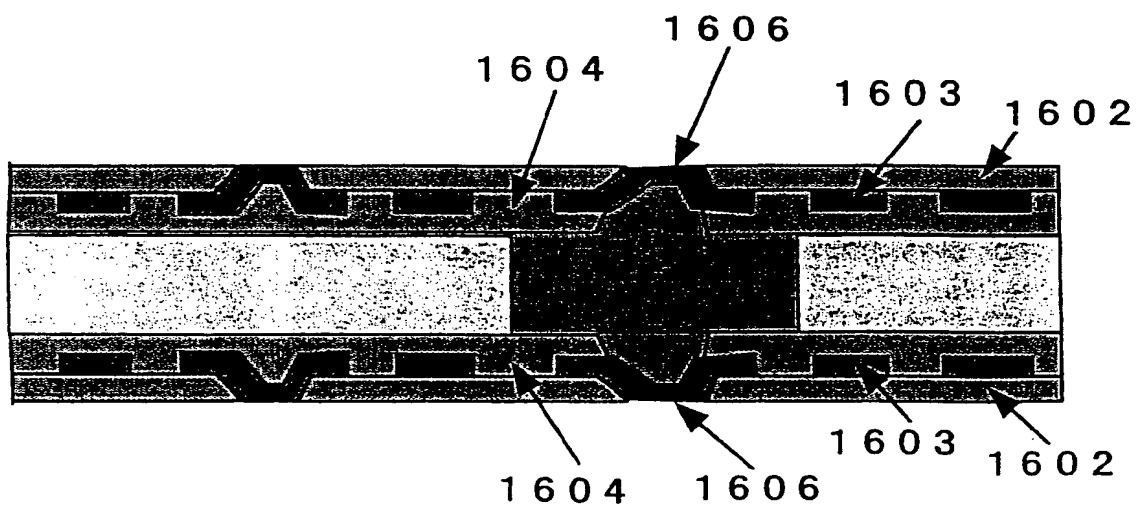
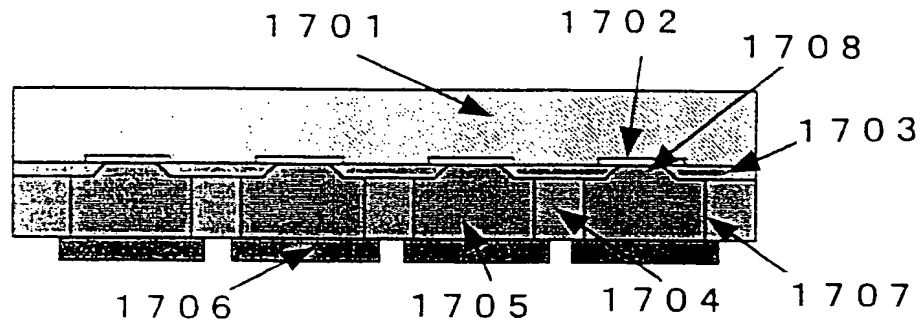


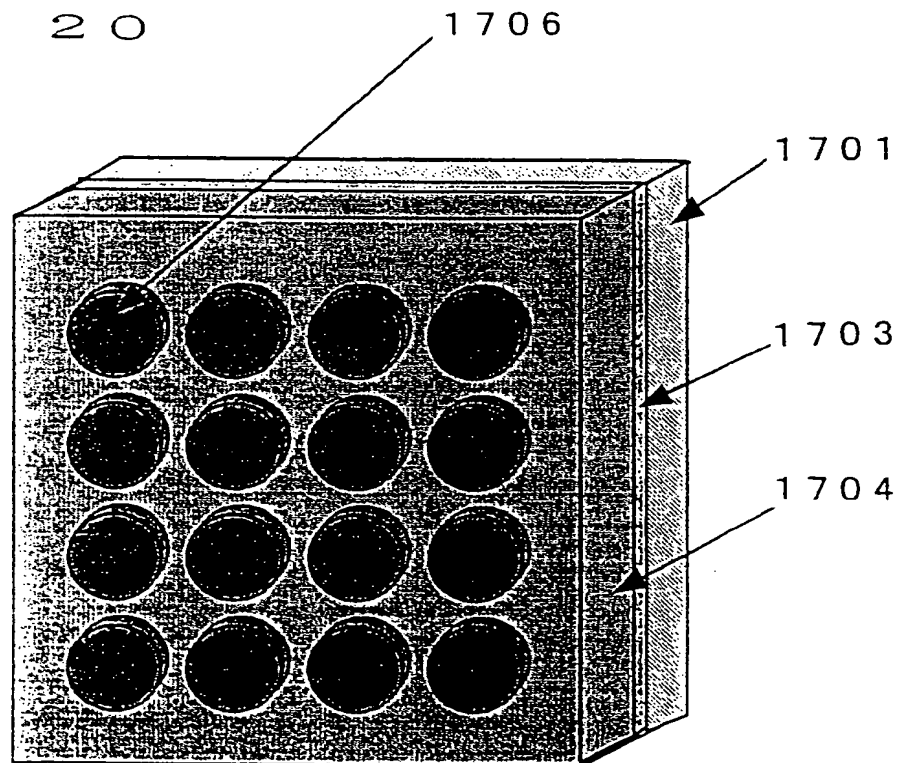
Fig. 18



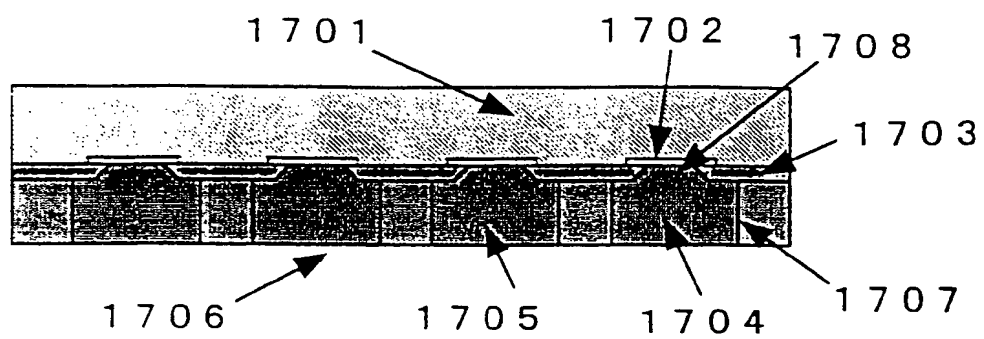
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F i g . 2 0



F i g . 2 1



(19)



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(11)

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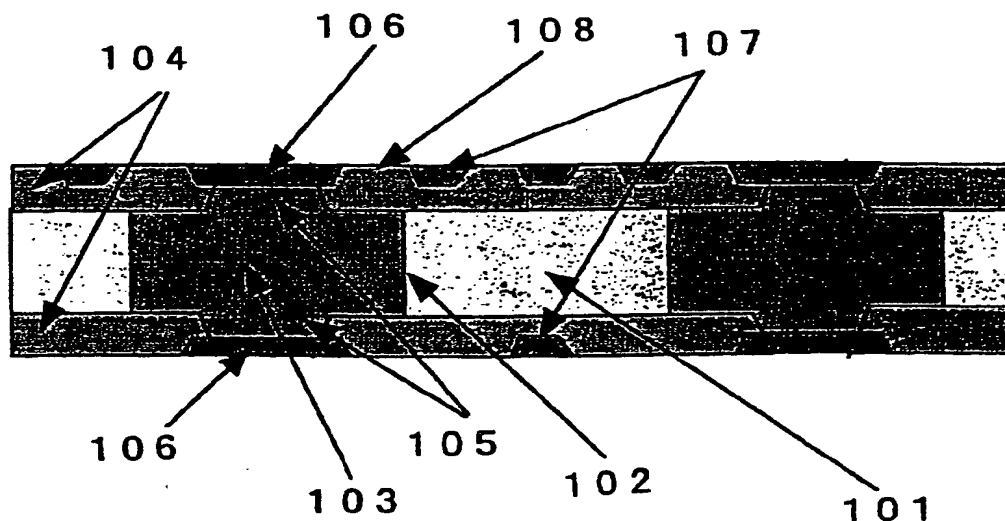
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(54) Printed circuit board and electric components

(57) A printed circuit board has: a base material layer (101) having a first via hole (103); and an insulating layer (104) having a second via hole (105), the insulating layer (104) being provided on one surface of the base material layer (101), wherein a cross-sectional

area of the second via hole (105) is smaller than a cross-sectional area of said first via hole (103), and wherein the first and second via holes (103,105) are filled with a conductive material.

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EUROPEAN SEARCH REPORT

Application Number
EP 97 12 2824

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US 5 473 120 A (ITO ET AL.) 5 December 1995 (1995-12-05) * claims; figures *	1,5-8	H05K3/40 H05K3/46 H05K3/20 H01L23/498 H01L23/31 H01L21/60
Y	---	2,3	
A	EP 0 567 306 A (NIPPON CMK CORP.) 27 October 1993 (1993-10-27) * abstract; figures 3,11 *	1,6,20	
Y	---	2,3	
X	US 4 604 496 A (ISHIHARA ET AL.) 5 August 1986 (1986-08-05) * claims; figures *	1-3,6	
X	PATENT ABSTRACTS OF JAPAN vol. 13, no. 371 (E-807), 17 August 1989 (1989-08-17) & JP 01 124296 A (HITACHI CHEM CO), 17 May 1989 (1989-05-17) * abstract *	1,6,20	
X	PATENT ABSTRACTS OF JAPAN vol. 16, no. 322 (E-1233), 14 July 1992 (1992-07-14) & JP 04 093096 A (SHINKO ELECTRIC IND CO), 25 March 1992 (1992-03-25) * abstract *	1-3,5	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H05K H01L
A	PATENT ABSTRACTS OF JAPAN vol. 1996, no. 9, 30 September 1996 (1996-09-30) & JP 08 139450 A (TOSHIBA CORP), 31 May 1996 (1996-05-31) * abstract *	18	
X	EP 0 475 022 A (IBM) 18 March 1992 (1992-03-18) * the whole document *	21-24	
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 24 July 2000	Examiner Prohaska, G
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

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EUROPEAN SEARCH REPORT

Application Number
EP 97 12 2824

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Y	US 5 543 585 A (BOOTH RICHARD B ET AL) 6 August 1996 (1996-08-06) * the whole document *	12-17	
Y	EP 0 704 899 A (NIPPON ELECTRIC CO) 3 April 1996 (1996-04-03) * column 8, line 20 - column 16, line 54; figures 8,11,16G *	12-17	
A	PATENT ABSTRACTS OF JAPAN vol. 013, no. 513 (E-847), 16 November 1989 (1989-11-16) & JP 01 207938 A (NEC CORP), 21 August 1989 (1989-08-21) * abstract *	12-17	
A	US 5 473 194 A (TANAKA MINORU ET AL) 5 December 1995 (1995-12-05)		
A	PATENT ABSTRACTS OF JAPAN vol. 012, no. 167 (E-610), 19 May 1988 (1988-05-19) & JP 62 277754 A (HITACHI CHEM CO LTD), 2 December 1987 (1987-12-02)		
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 24 July 2000	Examiner Prohaska, G
<p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document</p>			

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Application Number

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CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

- ☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):
- ☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

- ☒ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.
- ☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.
- ☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:
- ☐ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:



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**LACK OF UNITY OF INVENTION
SHEET B**

Application Number
EP 97 12 2824

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims: 1-11, 18-20

Printed circuit board

2. Claims: 12-17, 21-25

Component package

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 97 12 2824

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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24-07-2000

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5473120 A	05-12-1995	CA 2094754 A	28-10-1993
		JP 6232560 A	19-08-1994
EP 567306 A	27-10-1993	JP 5299844 A	12-11-1993
		JP 6164148 A	10-06-1994
		JP 6164149 A	10-06-1994
US 4604496 A	05-08-1986	JP 1579402 C	13-09-1990
		JP 2005315 B	01-02-1990
		JP 60047495 A	14-03-1985
		DE 3428259 A	14-03-1985
JP 01124296 A	17-05-1989	NONE	
JP 04093096 A	25-03-1992	NONE	
JP 08139450 A	31-05-1996	NONE	
EP 0475022 A	18-03-1992	US 5086558 A	11-02-1992
		JP 1975631 C	27-09-1995
		JP 4234139 A	21-08-1992
		JP 6080703 B	12-10-1994
US 5543585 A	06-08-1996	JP 2596721 B	02-04-1997
		JP 7231011 A	29-08-1995
		US 5747101 A	05-05-1998
EP 0704899 A	03-04-1996	JP 2581017 B	12-02-1997
		JP 8102474 A	16-04-1996
		CA 2159243 A	31-03-1996
		CN 1128901 A	14-08-1996
		US 5897337 A	27-04-1999
JP 01207938 A	21-08-1989	NONE	
US 5473194 A	05-12-1995	JP 2633366 B	23-07-1997
		JP 3165054 A	17-07-1991
JP 62277754 A	02-12-1987	NONE	

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82